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10/784,918	02/24/2004	Naoki Takada	62807-166	1966

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EXAMINER
SHERMAN, STEPHEN G

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2629	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/03/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/784,918	TAKADA ET AL.	
	Examiner	Art Unit	
	Stephen G. Sherman	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 4-13, 17 and 20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The claims all recite the limitations such as "...the second clock not being created every n signal creation..." or "...the scan driver selects pixels of n rows a plurality of times..." or "...using blanking data once per n lines of the pixel array..." These limitations render the claims indefinite because n is not defined in the claims. As such in the case of "...the second clock not being created every n signal creation..." what if n=o, then the clock signal would always be created and black data would never be supplied, or what if n=1, then the clock signal would never be created and the black data would always be supplied. Neither of these situations is in line with what the invention of the applicant is and thus the claim fails to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Similar situations arise with the limitations "...the scan driver selects pixels of n rows a plurality of times..." and "...using blanking data once per n lines of the pixel array..." For the purposes of

examination, the examiner will interpret that in all cases n is not zero, and that the value of n corresponds with the values that the applicant has given in their specification.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-3 and 14-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Arimoto et al. (US 2003/00090449).

Regarding claim 1, Arimoto et al. disclose a display device, comprising:

a pixels array including a plurality of pixels arranged in a form of a matrix (Figure 21, LIQUID CRYSTAL PANEL 405);

a data driver for supplying a tone voltage corresponding to display data to the pixels (Figure 21, SOURCE DRIVER 403); and

a scan driver for supplying a gate signal to the pixels to select therefrom pixels to which the tone voltage is to be supplied (Figure 21, GATE DRIVER 404), wherein:

the scan driver selects first n rows (n > 2) of pixels (Figure 24 shows that the first 4 rows are the rows labeled as GATE PULSE P5 through GATE PULSE P8.), sequentially selects m rows (m n) of second n rows of pixels (Figure 24 shows that the second 4 rows labeled as GATE PULSE P1 through GATE PULSE P4 as selected sequentially.), and selects pixels from the second n rows of pixels a plurality of times for each row during one frame period (Figure 24 shows that during one frame period the lines GATE PULSE P1 through GATE PULSE P4 are each selected twice, each of the selection represented by a positive pulse.); and

the data driver supplies a tone voltage corresponding to black data to the first n rows of pixels (Figure 24 shows that the voltage supplied to the first 4 rows is for black data as explained in paragraph [0189].) and sequentially supplies the tone voltage corresponding to the display data to the second n rows of pixels (Figure 24 and paragraph [0189] explain that the second rows are sequentially selected and applied with voltages that correspond to image data.).

Regarding claim 2, Arimoto et al. disclose the display device according to claim 1, wherein:

the scan driver selects first four rows of pixels at a time, sequentially selects pixels from second four rows of pixels for each row, and selects pixels from the second four rows of pixels twice for each row (As explained above in the rejection of claim 1, the rows are selected in groups of 4, and the second four rows are selected twice.); and

the data driver supplies the tone voltage corresponding to the black data to the first row of pixels at a time and sequentially supplies the tone voltage corresponding to the display data to the second four rows of pixels (As explained above in the rejection of claim 1, Figure 24 and paragraph [0189] explain that four rows are selected at a time and that the first group get black data and that the second four get image data.).

Regarding claim 3, Arimoto et al. disclose the display device according to claim 1, wherein when the gate signal to be supplied from the scan driver to pixels of a preceding row falls, the gate signal to be supplied from the scan driver to pixels of a succeeding row rises (Figure 24 shows that as the gate pulse GATE PULSE P2 falls, the gate pulse GATE PUSLE P3 rises.).

Regarding claim 14, Akimoto et al. disclose a display device, comprising:

a pixels array including a plurality of pixels arranged in a form of a matrix (Figure 4, LIQUID CRYSTAL PANEL 405);

a data driver for supplying a tone voltage corresponding to display data to the pixels (Figure 4, SOURCE DRIVER 403);

a scan driver for selecting pixels of at least one row to which the tone voltage is to be supplied (Figure 4, GATE DRIVER 404); and

a control circuit for controlling the data driver and the scan driver (Figure 4, SIGNAL CONVERTING SECTION 401 and DRIVING PULSE GENERATING SECTION 402 make up the control circuit.), wherein:

the control circuit outputs a first clock signal and the display data to the data driver (Figures 4-5 and paragraph [0018], where SIGNAL CONVERTING SECTION 401 outputs the image data to the SOURCE DRIVER 403 and the DRIVING PULSE GENERATING SECTION 402 outputs the SOURCE DRIVER CONTROL SIGNAL, i.e. a clock signal to the SOURCE DRIVER 403.);

the control circuit outputs to the scan driver a second clock signal synchronized with the first clock signal and a scanning start signal generated a plurality of times during one frame period (Figure 4 shows that the DRIVING PULSE GENRATING SECTION 402 outputs a GATE DRIVER CONTROL SIGNAL to the GATE DRIVER 404, where this signal would contain pulses for controlling the driver, i.e. clock signals, where it is inherent that there would be a scanning start signal, and as explained in paragraph [0019], the POLARITY CONTROL SIGNAL, i.e. clock signal, is generated by the DRIVING PULSE GENRATING SECTION 402.); and

the control circuit outputs to the data driver blanking data other than the display data in place of the display data during a second half of a period the second clock signal (Figure 7 shows that the POLARITY CONTROL SIGNAL has a period which starts positive and then goes negative until the period is over and the signal repeats. During the second half of this signal, i.e. when the signal is negative, the display data other than the display data, as indicated in the Figure by the pulses with a B next to them, is outputted. This can be shown by looking at the first time the POLARITY CONTROL SIGNAL goes negative in the Figure. During this negative portion, the GATE PULSE P7 supplied a pulse of negative polarity which corresponds no non-display data, and

therefore blanking data other than the display data is outputted during a second half of the clock signal.).

Regarding claim 15, Akimoto et al. disclose the display device according to claim 14, wherein the period of the first and second clock signals is two horizontal scanning periods (Figure 7 shows that the period of the POLARITY CONTROL SIGNAL represents two clocks of the DOUBLE-SPEED SIGNAL.).

Regarding claim 16, Akimoto et al. disclose a display device according to claim 15, wherein:

the scan driver sequentially selects the pixels of one row in response to the second clock signal during a first half of the period of the second clock signal (Figure 7 shows that the rows are sequentially selected in accordance with the POLARITY CONTROL SIGNAL, where they are sequentially selected during the first period as shown by the positive pulses.) and selects the pixels twice for each row at a period of one frame in response to the scanning start signal (Figure 7 shows that during one frame period, where the start scanning signal would determine the start of the frame periods, that each row is selected twice as shown by the two pulse of positive and negative polarity.); and

the scan driver sequentially selects the pixel of one row in response to the second clock signal during a second half of the period of the second clock signal (Figure 7 shows that the rows are sequentially selected in accordance to the POLARITY

CONTROL SIGNAL, where they are sequentially selected during the second period as shown by the negative pulses.).

Regarding claim 17, Arimoto et al. disclose a display device, comprising:

a pixels array including a plurality of pixels arranged in a form of a matrix (Figure 21, LIQUID CRYSTAL PANEL 405);

a data driver for supplying a tone voltage corresponding to display data to the pixels (Figure 21, SOURCE DRIVER 403); and

a scan driver for supplying a gate signal to the pixels to select therefrom pixels to which the tone voltage is to be supplied (Figure 21, GATE DRIVER 404), wherein:

the scan driver selects the pixels of n rows a plurality of times for each row during one frame period (Figure 24 shows that the gate lines corresponding to GATE PUSLE P1 through GATE PULSE P4 are each selected twice, each of the selection represented by a positive pulse.).

Regarding claim 18, Arimoto et al. disclose a display device, comprising:

a pixels array including a plurality of pixels arranged in a form of a matrix (Figure 4, LIQUID CRYSTAL PANEL 405);

a data driver for supplying a tone voltage corresponding to display data to the pixels (Figure 4, SOURCE DRIVER 403); and

a scan driver for supplying a gate signal to the pixels to select therefrom pixels to which the tone voltage is to be supplied (Figure 4, GATE DRIVER 404), wherein:

the scan driver selects the pixels a plurality of times for each row during one frame period (Figure 7 shows that all of the gate lines corresponding to GATE PUSLE P1 through GATE PULSE P10 are each selected twice, one of the selections represented by a positive pulse the other by a negative pulse.); and

the data driver supplies to the pixels a tone voltage corresponding to black data in place of the display data at a predetermined interval of time (Figure 7 shows that according to the DOUBLE-SPEED SIGNAL the black data applied to the gate lines in place of the image data at a predetermined interval of time.).

Regarding claim 19, Arimoto et al. disclose a display device, comprising:

a pixels array including a two-dimensional pixels including a plurality of pixels arranged in rows in a first direction and in columns in a second direction vertical to the first direction (Figure 15 LIQUID CRYSTAL PANEL 405);

a plurality of scanning signal lines for supplying a scanning signal to each group of pixels juxtaposed in the second direction (Figure 15 shows GL1 through GL11);

a plurality of data signal lines for supplying a data signal including a tone signal of display data to each group of pixels juxtaposed in the first direction (Figure 15 shows SL1 through SL10);

a scan driver for outputting the scanning signal to each of the scanning signal lines (Figure 15, GATE DRIVER 404);

a data driver for outputting the data signal to each of the data signal lines (Figure 15, SOURCE DRIVER 403); and

a control circuit for transmitting a first clock signal for the scanning driver to start scanning of the scanning signal lines and for transmitting a second clock signal controlling the display data transmitted to the data driver (Figure 15, DRIVING PULSE GENERATING SECTION 1502, which outputs SOURCE DRIVER CONTROL SIGNAL and GATE DRIVER CONTROL SIGNAL to the source and gate drivers, respectively. Refer to paragraphs [0150]-[0160].), wherein:

the control circuit outputs the scanning signal from the scanning driver twice to selected lines selected from the lines of the pixels array, the number of the selected lines being less than that of the lines of the pixels array (Figure 16 shows that each of the lines being selected is less than the total number of lines, and where the first selection of the gate line corresponding to GATEPULSE P1 occurs twice.);

the control circuit outputs the scanning signal from the scanning driver three times during one frame period (Figure 16 shows that the gate lines are all selected three times during the frame period as shown by the three positive pulses applied to every gate line.); and

the control circuit outputs the display data and data indicating a black tone to the data driver during one frame period (Figure 16 shows that display data and black data are alternately applied according to the DOUBLE-SPEED SIGNAL.).

Regarding claim 20, Arimoto et al. disclose a method of driving a liquid crystal display device having a hold-type luminance response characteristic, comprising the steps of:

changing the hold-type luminance response characteristic into an impulse-type luminance response characteristic by masking video data outputted to a pixels array of the display device using blanking data once per n lines of the pixels array (Figure 7 shows that black data is outputted once per n lines of the array, which is controlled by the DOUBLE-SPEED SIGNAL, where the black data is shown in the Figure by a B next to the pulse.); and

outputting twice during one frame period a gate signal to a gate line corresponding to each pixel row of the pixels array (Figure 7 shows that during one frame period the all of the lines GATE PULSE P1 through GATE PULSE P10 are each selected twice, one of the selections represented by a positive pulse and the other represented by a negative pulse.).

5. Claims 4-13 are rejected under 35 U.S.C. 102(e) as being anticipated by Nitta et al. (US 7,027,018)

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Regarding claim 4, Nitta et al. disclose a display device, comprising:

a pixels array including a plurality of pixels arranged in a form of a matrix (Figure 3, item 101 is explained to be a pixel array in column 11, lines 61-65.);

a data driver for supplying a tone voltage corresponding to display data to the pixels (Figure 3, item 102 is explained to be data driver in column 12, lines 48-51.);

a scan driver for selecting pixels of at least one row to which the tone voltage is to be supplied (Figure 3, items 103-1 through 103-3 are explained to the scanning drivers in column 12, lines 51-55.); and

a control circuit for controlling the data driver and the scan driver (Figure 3, item 104 which is explain in column 12, lines 61-67.), wherein:

the control circuit outputs a first clock signal and the display data to the data driver (Figure 3 and column 12, lines 61-67 explain that timing signals 107 and display data 1056 are supplied from the control circuit 104 to the data driver 102.);

the control circuit outputs to the scan driver a second clock signal, the second clock signal not being created every n signal creation thereof and outputs a scanning start signal generated a plurality of times during one frame period (Figure 3 shows that the control circuit 104 outputs a clock CL3 labeled as 112 to the scanning drivers 103-1 through 103-3. Figure 4 shows that the clock CL3 is not created every 5^{th} signal creation. Column 12, lines 61-67 that the scanning start signal 113 labeled as FLM in the Figures is also outputted by the control circuit 104 to the scanning drivers 103-1 through 103-3.); and

the control circuit outputs to the data driver blanking data other than the display data in place of the display data at timing at which the second clock signal is not created

(Figure 4 shows that when blanking data labeled as B in the O-DDR signal is supplied to the gate lines such as G1-G4, that the clock CL3 is not created.).

Regarding claim 5, Nitta et al. disclose the display device according to claim 4, further comprising:

a first memory to keeping the display data therein (Column 15, lines 15-25 explain that memory 105 is used to store the display data.); and

a second memory for keeping the blanking data therein (Column 15, lines 25-29 explain that the blanking data are stored in the pixels array, i.e. a second memory different from memory 105.), wherein:

the control circuit reads the display data from the first memory at timing synchronized with the first clock signal, outputs the display data to the data driver, reads the blanking data from the second memory at timing which is synchronized with the first clock signal and at which the second clock signal is not created, and outputs the blanking data to the data driver (As explained above, display data is output in accordance with the clock CL1 and would be output from memory 105, while the blanking data would be output when clock CL3 is not created and would be read from the place where it is stored in the pixel array.).

Regarding claim 6, Nitta et al. disclose the display device according to claim 4, wherein a period of the first clock signal and a period of the second clock signal are synchronized with a scanning period for the scan driver to select pixels of at least one of

the rows of pixels (Figure 4 shows that the period of clocks CL1 and CL3 are synchronized with the scan driver for producing the selection of pixels as shown by the pulses on gate lines GL1 through G516 in the Figure.).

Regarding claim 7, Nitta et al. disclose the display device according to claim 4, wherein:

the scan driver sequentially selects one row of pixels in response to the second clock signal and selects the pixels twice for each row at a period of one frame in response to the scanning start signal (Figure 4 shows that that the gate lines are sequentially selected according to clock signal CL1 and Figure 10 shows that each gate line is selected twice in a frame period, as indicated by the two gate pulses.);

the scan driver selects n rows of pixels at timing at which the second clock signal is not created (Figure 4 shows that 4 rows are selected when clock signal CL3 is not created.);

the data driver supplies the tone voltage corresponding to the display data to the pixels of one row in response to the first clock signal (Figure 4 shows that in accordance with clock signal CL1 display data is supplied one row at a time to rows G513 through G516.); and

the data driver supplies the tone voltage corresponding to the blanking data to the pixels of n rows (Figure 4 shows that blanking data B shown in signal O-DDR is supplied to the 4 rows G1 through G4.).

Regarding claim 8, Nitta et al. disclose the display device according to claim 4, wherein the control circuit outputs to the scan driver a first scanning enable signal to invalidate selection of the pixels by the scan driver at timing at which the second clock signal is not created and a second scanning enable signal to validate selection of the pixels by the scan driver at timing at which the second clock signal is not created (Figure 4 shows signals DISP1 through DISP3. Column 24, lines 3-25 explain that DISP1 makes it possible to validate selection of pixels by the scan driver when CL3 is not created, where as signals DISP2 and DISP3 invalidate the selection during the period when CL3 is not created).

Regarding claim 9, Nitta et al. disclose a display device, comprising:

a pixels array including a plurality of pixels arranged in a form of a matrix (Figure 3, item 101 is explained to be a pixel array in column 11, lines 61-65.);

a data driver for supplying a tone voltage corresponding to display data to the pixels (Figure 3, item 102 is explained to be data driver in column 12, lines 48-51.);

a scan driver for selecting pixels of at least one row to which the tone voltage is to be supplied (Figure 3, items 103-1 through 103-3 are explained to the scanning drivers in column 12, lines 51-55.); and

a control circuit for controlling the data driver and the scan driver (Figure 3, item 104 which is explain in column 12, lines 61-67.), wherein:

the control circuit outputs a first clock signal and the display data to the data driver (Figure 3 and column 12, lines 61-67 explain that timing signals 107 and display data 1056 are supplied from the control circuit 104 to the data driver 102.);

the control circuit outputs to the scan driver a second clock signal, the second clock signal not being created every n signal creation thereof (Figure 3 shows that the control circuit 104 outputs a clock CL3 labeled as 112 to the scanning drivers 103-1 through 103-3. Figure 4 shows that the clock CL3 is not created every 5th signal creation.), a first scanning enable signal to invalidate selection of the pixels by the scan driver at timing at which the second clock signal is not created, and a second scanning enable signal to validate selection of the pixels by the scan driver at timing at which the second clock signal is not created (Figure 4 shows signals DISP1 through DISP3. Column 24, lines 3-25 explain that DISP1 makes it possible to validate selection of pixels by the scan driver when CL3 is not created, where as signals DISP2 and DISP3 invalidate the selection during the period when CL3 is not created); and

the control circuit outputs to the data driver predetermined data other than the display data in place of the display data at timing at which the second clock signal is not created (Figure 4 shows that when blanking data labeled as B in the O-DDR signal is supplied to the gate lines such as G1-G4, that the clock CL3 is not created.).

Regarding claim 10, Nitta et al. disclose the display device according to claim 9, wherein the control circuit outputs to the scan driver a signal once at a period of one frame, the signal having time width of a period of time from a first point of timing at

which the second clock signal is not created to a second next point of timing at which the second clock signal is not created (Figure 4 shows that FLM and DISP1 have a width that corresponds from when clock CL3 is not created to the next time CL3 is not created.).

Regarding claim 11, Nitta et al. disclose a display device, comprising:

a pixels array including a plurality of pixels arranged in a form of a matrix (Figure 3, item 101 is explained to be a pixel array in column 11, lines 61-65.);

a data driver for supplying a tone voltage corresponding to display data to the pixels (Figure 3, item 102 is explained to be data driver in column 12, lines 48-51.);

a scan driver for selecting pixels of at least one row to which the tone voltage is to be supplied (Figure 3, items 103-1 through 103-3 are explained to the scanning drivers in column 12, lines 51-55.); and

a control circuit for controlling the data driver and the scan driver (Figure 3, item 104 which is explain in column 12, lines 61-67.), wherein:

the control circuit outputs a first clock signal and the display data to the data driver (Figure 3 and column 12, lines 61-67 explain that timing signals 107 and display data 1056 are supplied from the control circuit 104 to the data driver 102.);

the control circuit outputs to the scan driver a second clock signal, the second clock signal not being created every n signal creation thereof and outputs a scanning start signal generated a plurality of times during one frame period (Figure 3 shows that the control circuit 104 outputs a clock CL3 labeled as 112 to the scanning drivers 103-1

through 103-3. Figure 4 shows that the clock CL3 is not created every 5th signal creation. Column 12, lines 61-67 that the scanning start signal 113 labeled as FLM in the Figures is also outputted by the control circuit 104 to the scanning drivers 103-1 through 103-3.); and

the control circuit outputs to the data driver blanking data other than the display data in place of the display data at timing at which the second clock signal is created immediately before the timing at which the second clock signal is not created (As shown in Figure 4, the point in time in which data B on O-DDR is supplied is immediately before the time when clock CL3 would be created.).

Regarding claim 12, Nitta et al. disclose the display device according to claim 11, wherein:

the scan driver selects the pixels of one row in response to the second clock signal and the scanning start signal during a period of time from a horizontal scanning period starting at timing at which the second clock signal is created immediately before the timing at which the second clock signal is not created to a horizontal scanning period starting at timing at which the second clock signal is not created (Figure 4 shows that before CL3 is not created that FLM is supplied and lines G513 through G56 are selected before CL3 is not created.); and

the scan driver selects the pixels of n rows during one horizontal scanning period at which the second clock signal is created immediately before the timing at which the

second clock signal is not created (Figure 4 shows that 4 rows G1 through G4 are selected immediately before CL3 is not created.).

Regarding claim 13, Nitta et al. disclose the display device according to claim 12, wherein:

the data driver supplies to the pixels the tone signal corresponding to the display data in response to the first clock signal during a horizontal scanning period starting at timing at which the second clock signal is created immediately before the timing at which the second clock signal is not created (Figure 4 shows that O-DDR has display data that is supplied during a time before CL3 is not created); and

the data driver supplies to the pixels the tone signal corresponding to the blanking data during a horizontal scanning period starting at timing at which the second clock signal is not created (Figure 4 shows that O-DDR has blanking data B that is supplied during a time when CL3 is not created.).

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Park et al. (US 2002/0084959) disclose a method of driving a liquid crystal display where a clock signal is applied to a gate driver along with three output enable

signals, and image data and black data are supplied to the display panel to prevent a motion blur.

Nose et al. (JP 2001-166280 A) disclose a driving method for a liquid crystal display in which multiple gate lines can be selected at the same time in accordance with clock and output enable signals.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen G. Sherman whose telephone number is (571) 272-2941. The examiner can normally be reached on M-F, 8:00 a.m. - 4:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SS

29 March 2007

AMR A. AWAD
SUPERVISORY PATENT EXAMINER